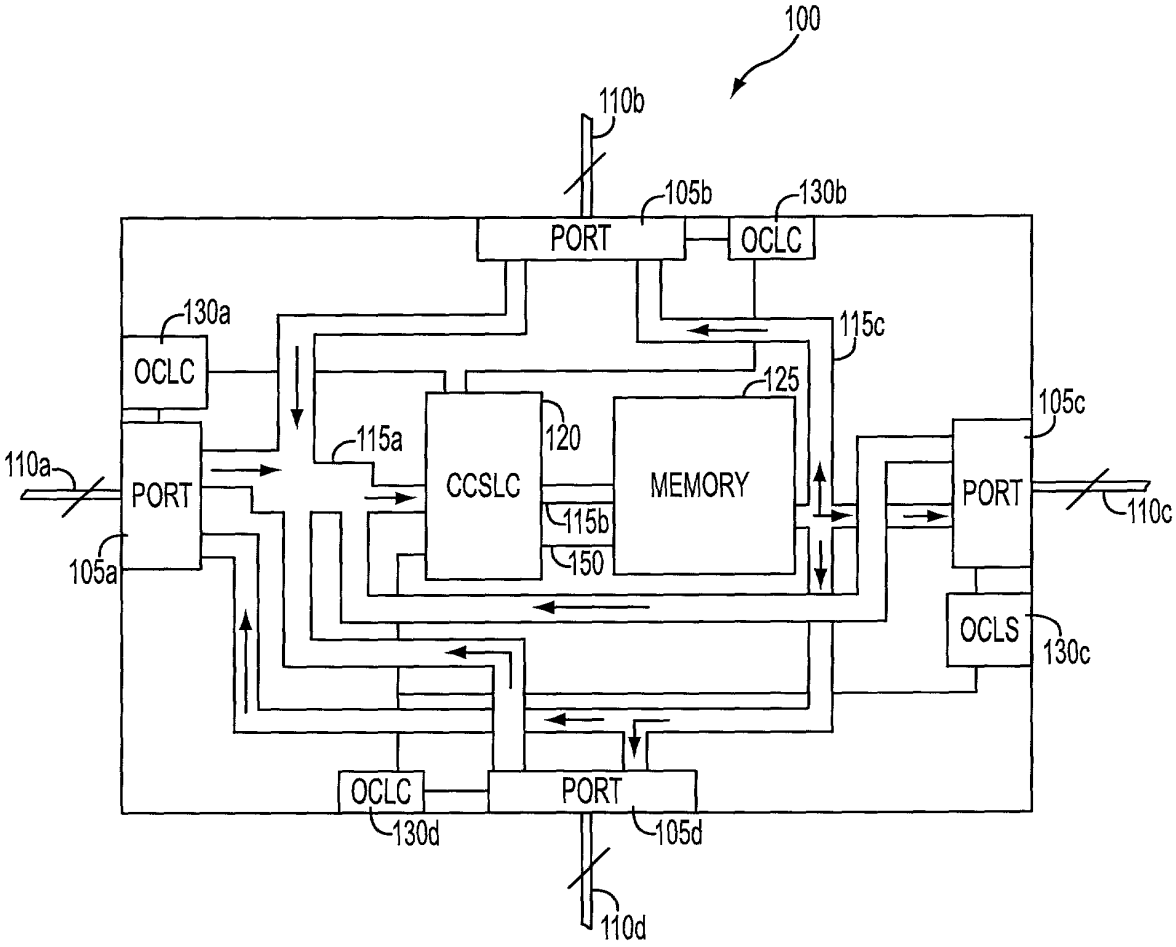
100
110b
105b
130b
PORT
OCLC
130a
OCLC
115c
125
105c
110a
PORT
115a
120
CCSLC
MEMORY
PORT
110c
115b
105a
150
OCLS
130c
OCLC
PORT
130d
105d
110d

FIG. 1

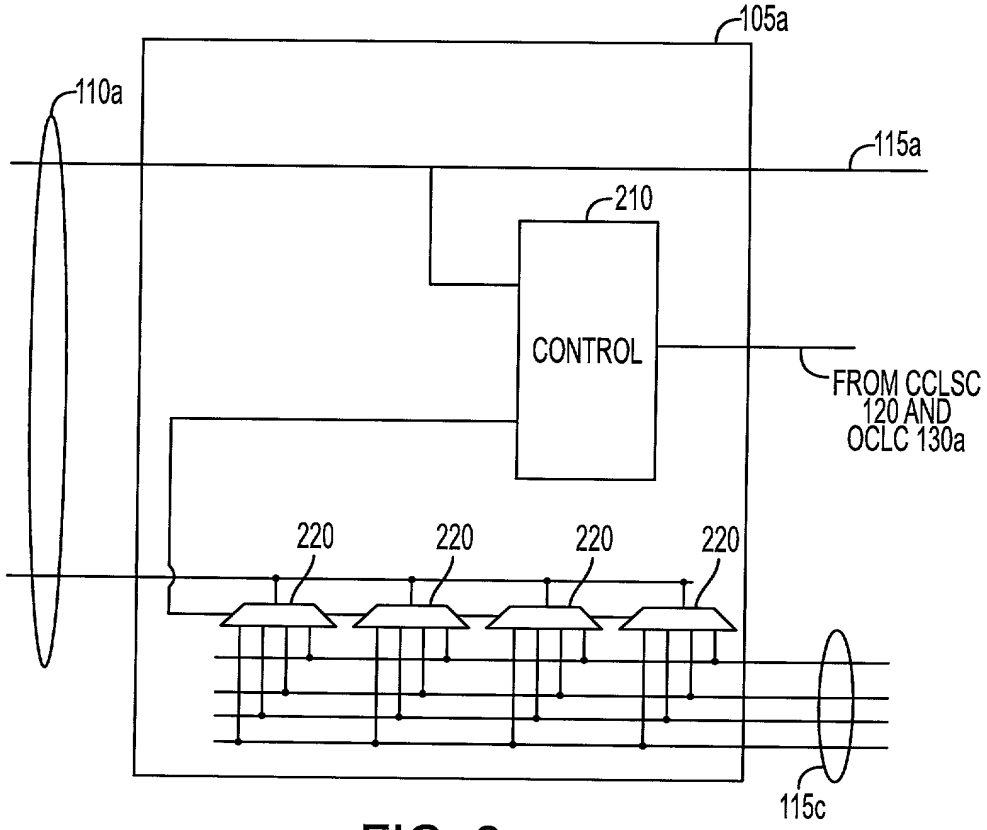
105a
110a
115a
210
CONTROL
FROM CCLSC
120 AND
OCLC 130a
220
220
220
220
115c

FIG. 2

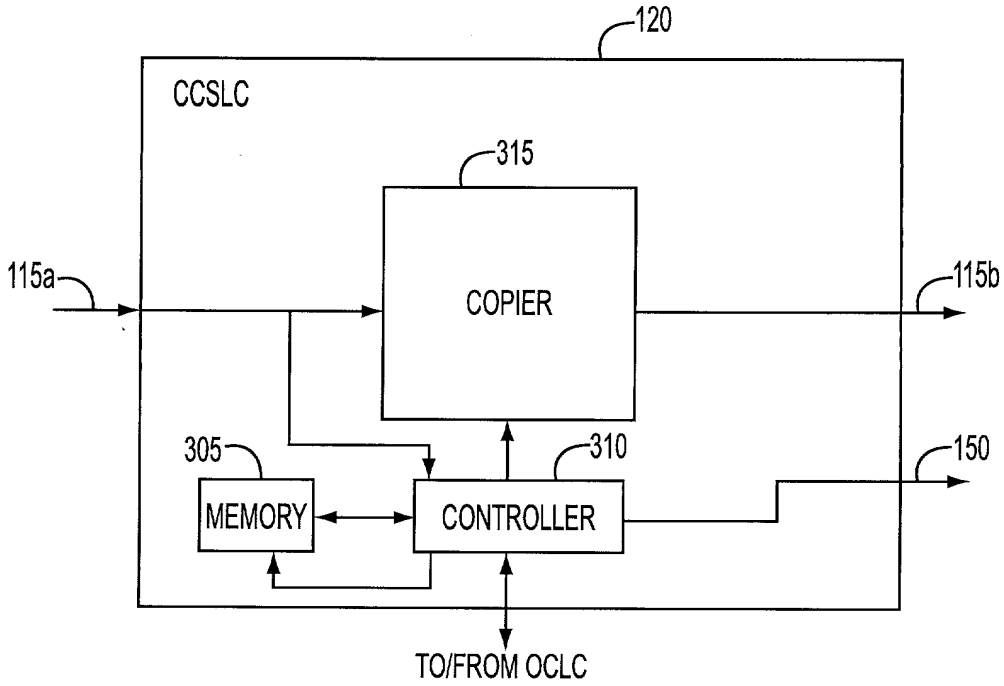
120
CCSLC
315
115a
COPIER
115b
305
310
150
MEMORY
CONTROLLER
TO/FROM OCLC

FIG. 3

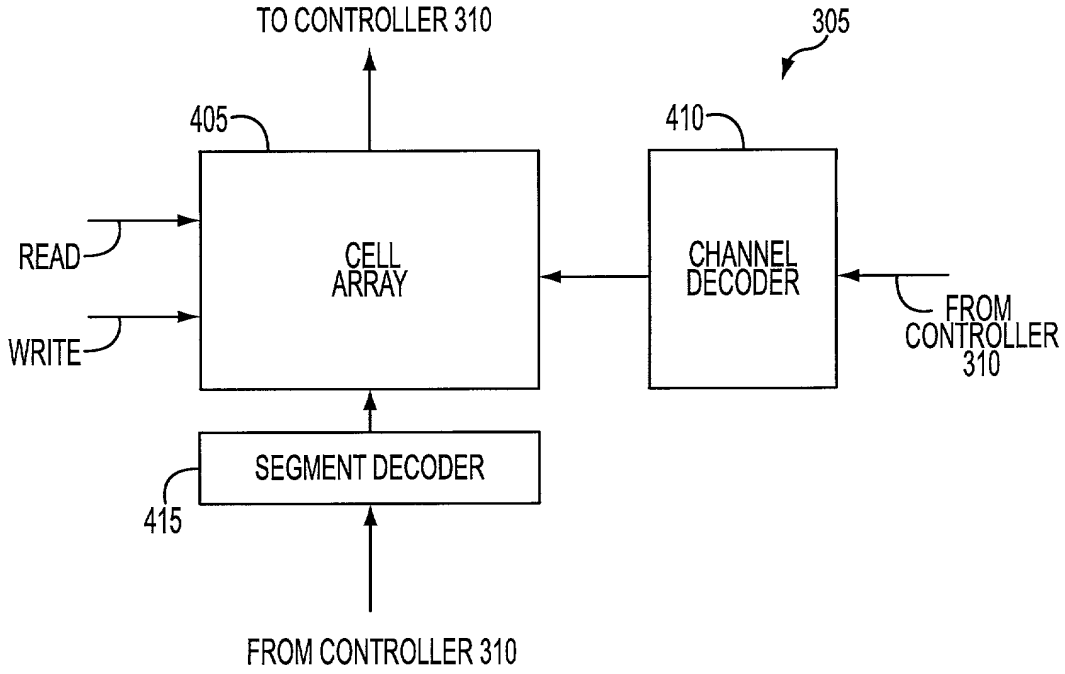
TO CONTROLLER 310
305
405
410
READ
WRITE
CELL ARRAY
CHANNEL DECODER
FROM CONTROLLER 310
SEGMENT DECODER
415
FROM CONTROLLER 310

FIG. 4a

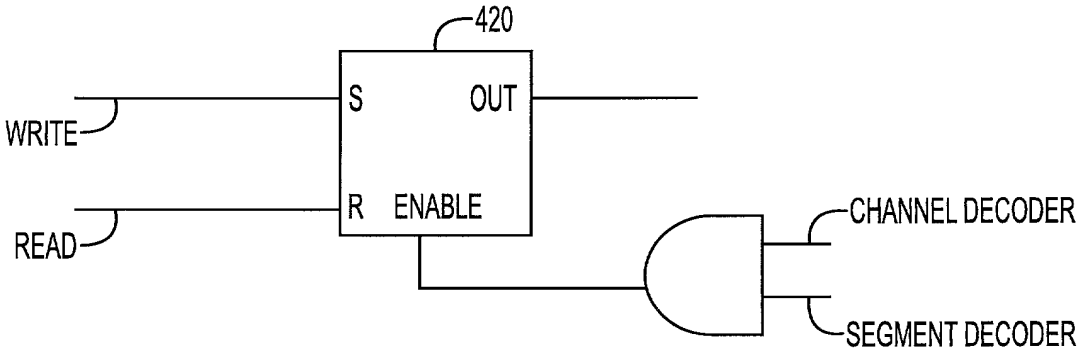
420
S
OUT
WRITE
R
ENABLE
READ
CHANNEL DECODER
SEGMENT DECODER

FIG. 4b

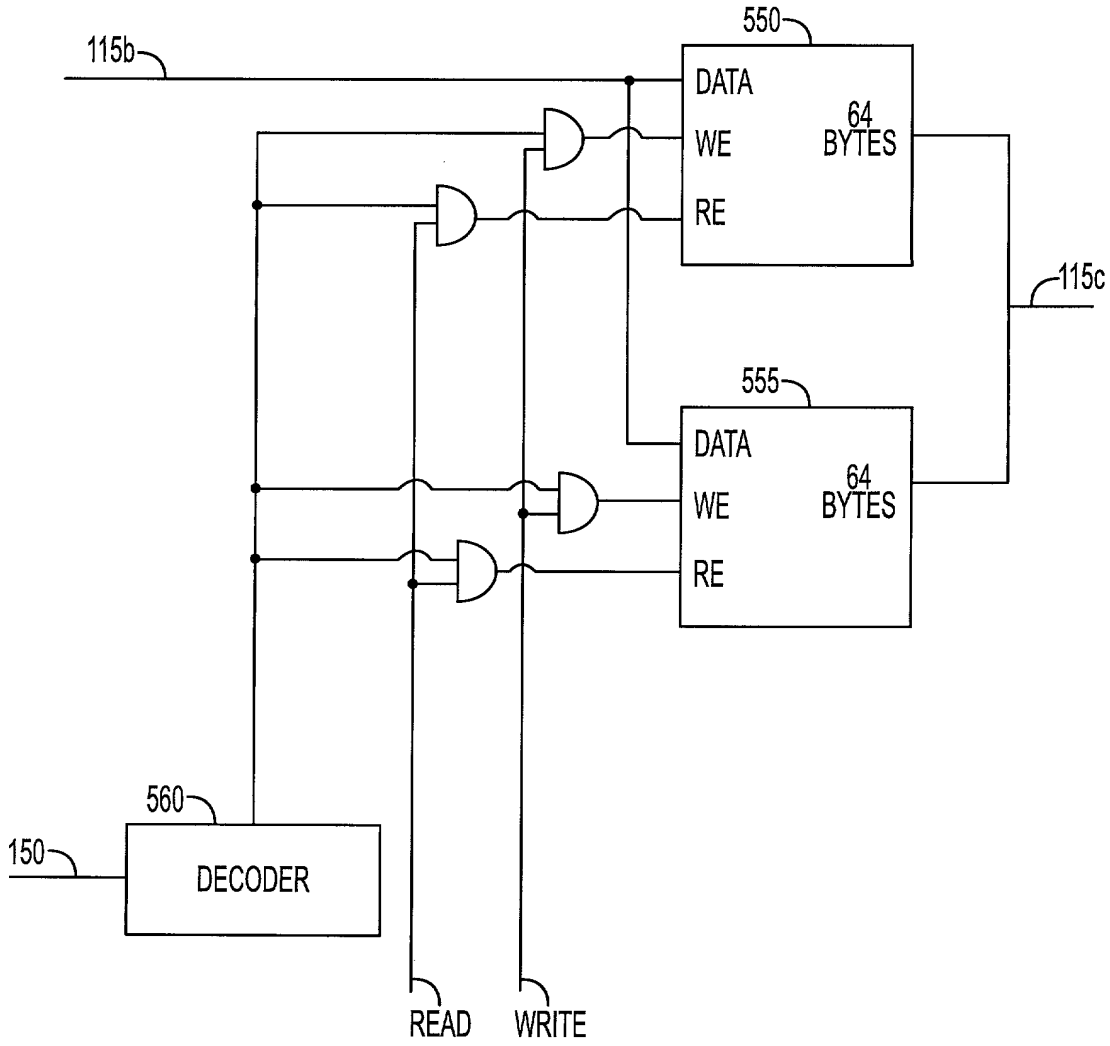
115b
550
DATA
WE
RE
64
BYTES
115c
555
DATA
WE
RE
64
BYTES
560
150
DECODER
READ
WRITE

FIG. 5

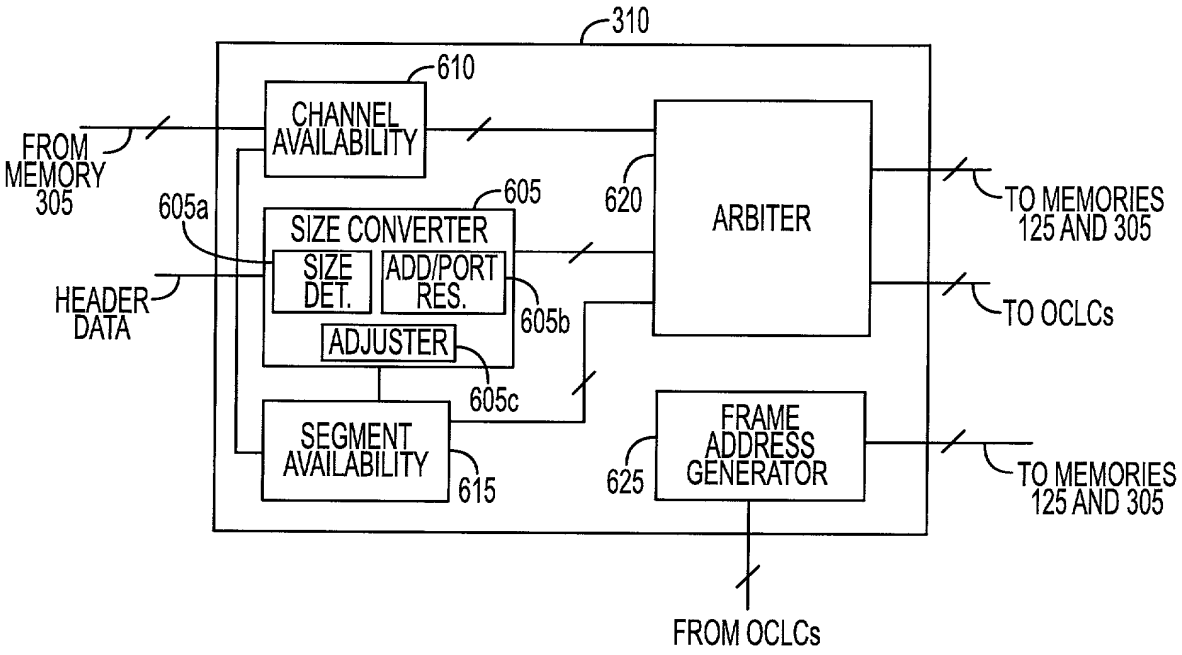
310
610
CHANNEL AVAILABILITY
FROM MEMORY 305
605a
605
SIZE CONVERTER
SIZE DET.
ADD/PORT RES.
605b
HEADER DATA
ADJUSTER
605c
620
ARBITER
TO MEMORIES 125 AND 305
TO OCLCs
SEGMENT AVAILABILITY
615
625
FRAME ADDRESS GENERATOR
TO MEMORIES 125 AND 305
FROM OCLCs

FIG. 6

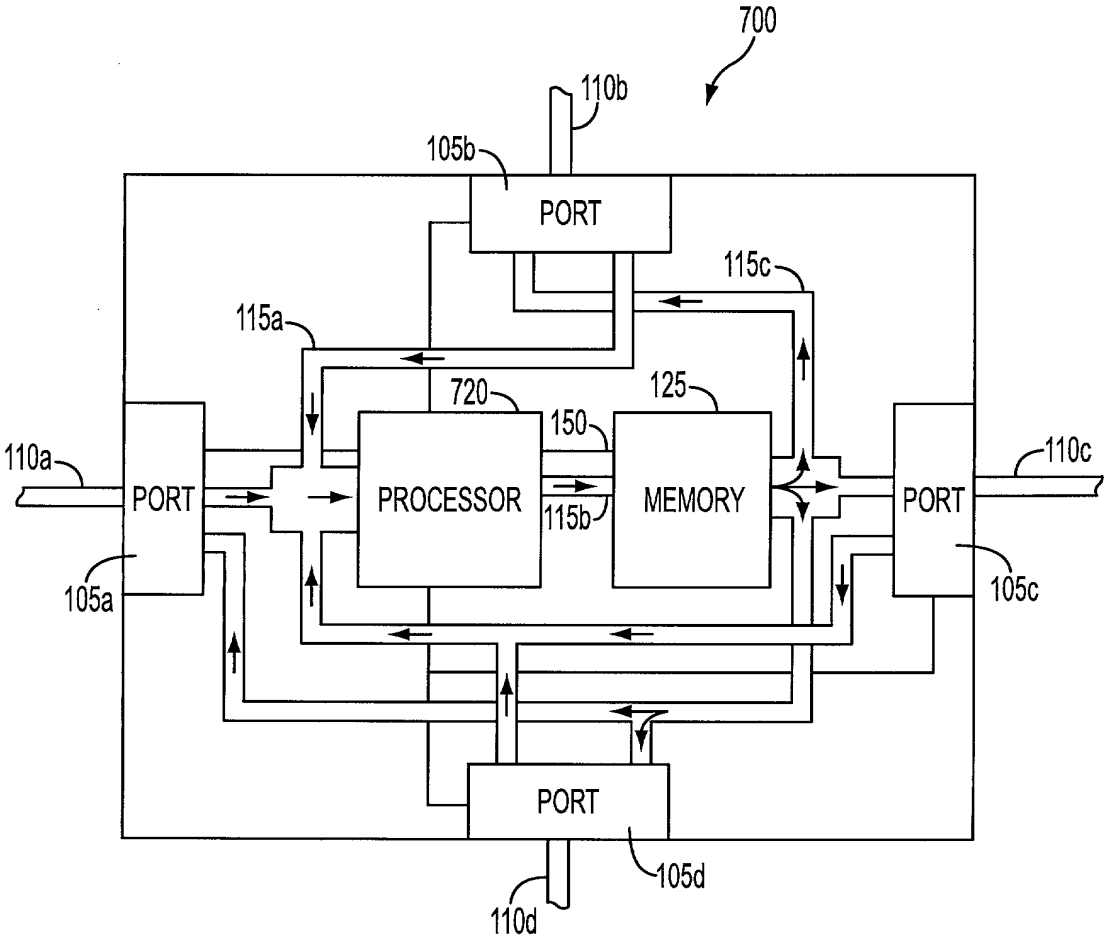
700
110b
105b
PORT
115c
115a
720
125
150
110a
PORT
PROCESSOR
MEMORY
PORT
110c
115b
105a
105c
PORT
105d
110d

FIG. 7

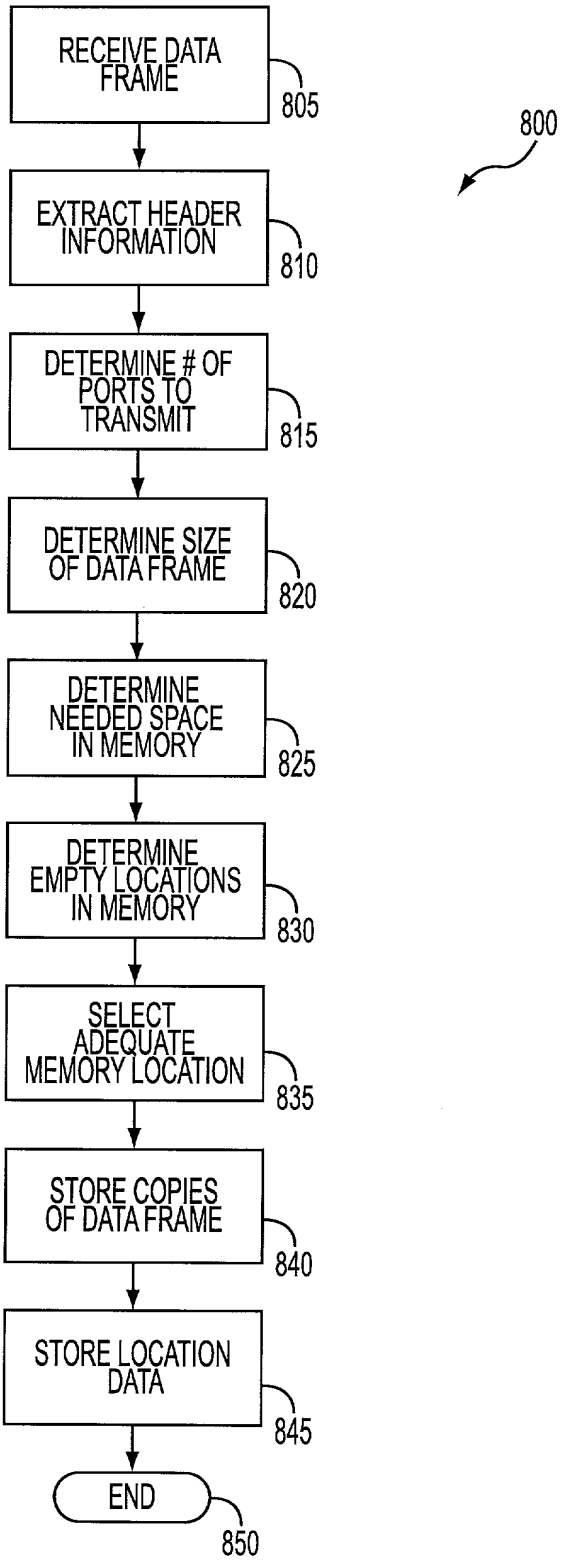
RECEIVE DATA FRAME
805
800
EXTRACT HEADER INFORMATION
810
DETERMINE # OF PORTS TO TRANSMIT
815
DETERMINE SIZE OF DATA FRAME
820
DETERMINE NEEDED SPACE IN MEMORY
825
DETERMINE EMPTY LOCATIONS IN MEMORY
830
SELECT ADEQUATE MEMORY LOCATION
835
STORE COPIES OF DATA FRAME
840
STORE LOCATION DATA
845
END
850

FIG. 8

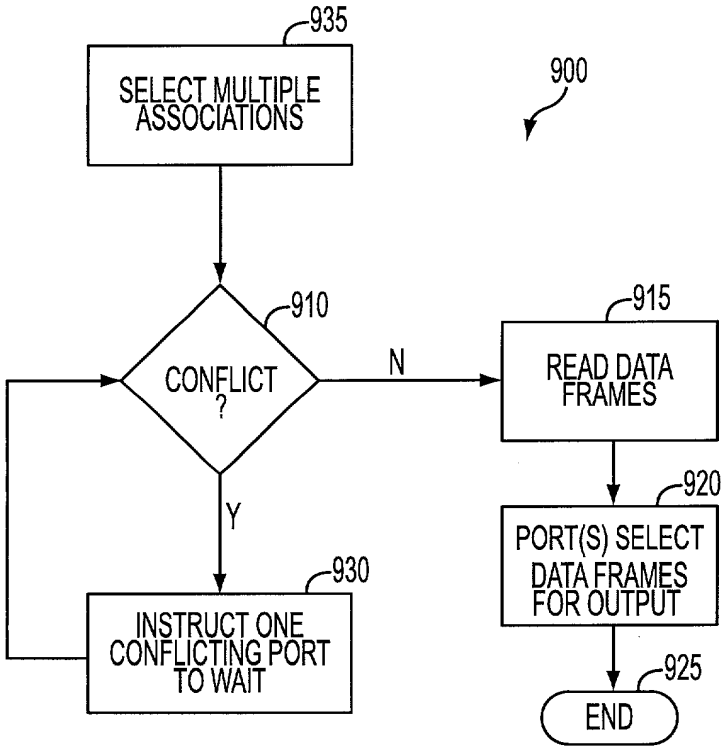
935
SELECT MULTIPLE ASSOCIATIONS
900
910
CONFLICT ?
N
915
READ DATA FRAMES
Y
920
PORT(S) SELECT DATA FRAMES FOR OUTPUT
930
INSTRUCT ONE CONFLICTING PORT TO WAIT
925
END

FIG. 9

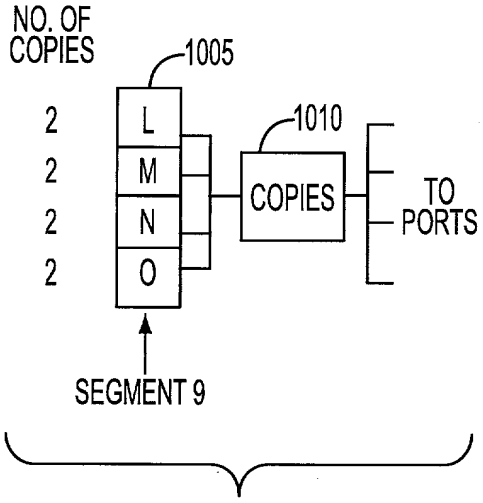

FIG. 10a

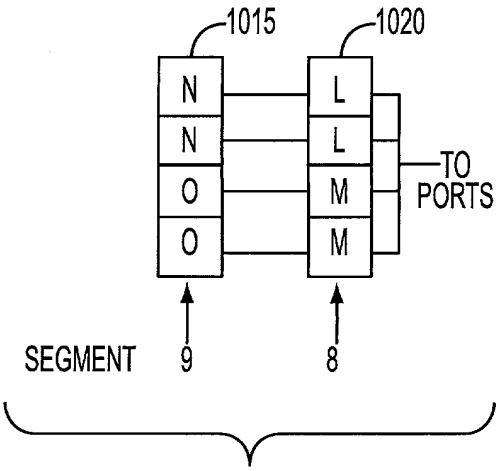

FIG. 10b

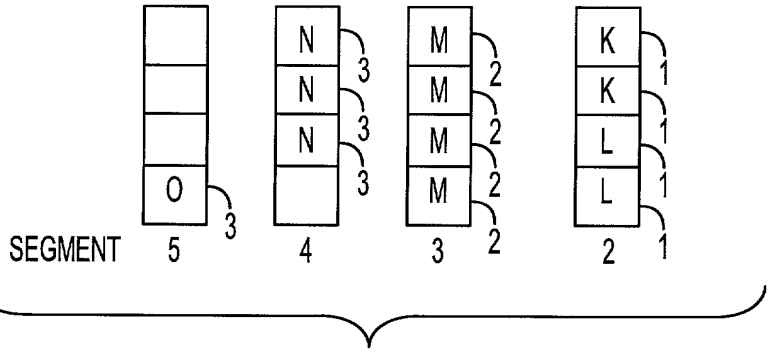

FIG. 10c